AMENDMENTS TO THE DRAWINGS

Four (4) sheets of replacement drawings showing labeling are attached for the Examiner's review.

Attachment: Replacement Sheet(s)

REMARKS

Claims 1-15 are all the claims pending in the application, claim 1 and new claims 13-15 being elected and claims 2-12 withdrawn from consideration. Reconsideration of the application and allowance of all claims are respectfully requested in view of the above amendments and the following remarks.

Replacement drawings are submitted concurrently with this amendment, adding descriptive labels to boxes that are not already labeled with well-understood functional symbols.

The objection to the disclosure is noted but is respectfully traversed. Fig. 4 illustrates the operation of the circuit 22 and is therefore accurately characterized in the Brief Description of the drawings. The D/A converter 22 does indeed operate as a window comparator. If the value of the digital signal is within a window, a 0 is output. If the value is above the window, a 1 is output, and if the value is below the window, a -1 is output. While window comparators often provide only binary outputs (i.e., between min and max or not between min and max), they also commonly deliver additional outputs indicating whether the input being analyzed is below the min or above the max. See, e.g., the window comparator described at http://www.acroname.com/brainstem/ref/h/Reflexes/rflxelem.html.

In any event, Brief Description of Fig. 4 and the detailed description at page 9 have both been amended for further clarity.

The anticipation rejection of claim 1 is respectfully traversed.

The D/A converter to which claim 1 is directed is shown in Fig. 1. Instead of having a single large D/A converter to convert the large input value, the circuit splits the D/A function

into four parts. Fig. 5 shows a filter structure wherein the input is divided by n and then passed to a 12-bit counter such that any of the twelve outputs of the counter 232 is a further division by 2^{12}. The 12-bit output from the counter 232 is passed through the 12-bit D/A converter 24 in Fig. 6. Instead of this, the circuit arrangement of Fig. 8 uses a divide-by-4 counter to distribute the output of counter 231 across four D/A converters which are separately converted and then used in connection with a respective plurality of varicap diodes as discussed in the second full paragraph of page 13 of the specification.

Spicer shows a D/A converter which includes two 16-bit D/A converters each receiving the same input. If there were only one D/A converter, there might be a glitch in the output when the input signal value changes. To avoid this, the changed input value is applied to a second D/A converter while the output of that D/A converter is not selected, and then the output of the second D/A converter can be selected after the glitch has passed. This is not the type of operation disclosed and claimed in the present case.

One clear difference between Spicer and the present invention resides in the manner in which continuous incrementing or decrementing is reflected at the D/A inputs. At a given point in time there would be a value in the counter 2325, and the four outputs from the counter 2325 will each increment at one fourth the rate of the input to counter 2325. These four outputs are each connected to a respective one of counters 2321 to 2324, so that when the counter 2325 increments by one, the value in counter D/A 2321 increments by one, when the value in counter 2325 increments again by one, the value in counter 2322 increments by one. When counter 2325 increments again, the value in counter 2323 increments, then 2324, then 2321, and so forth. So

for a continuous incrementing of the input values to the D/A converter circuit shown in Fig 8, the values in each of the counters 2321 to 2324 are incremented in turn, and this increments in turn the values at the inputs to the D/A converters 241 and 242, all as described in claim 1.

In Spicer, the "continuously incremented" value would be in the "suitable source" referred to at the top of column 3 of that specification, the source not being shown in the figures. When it increments by one, the incremented value is applied to D/A 10. When it increments again, this next incremented value is applied to the D/A 11. Note that this new value applied to the input of D/A 11 will be two increments above the last value applied to the D/A 11. Thus, there is no "divide-by" operation performed, and the result is that the D/A converters 10 and 11, though used alternately, must each be large enough to handle the full range of the values coming from the source. This does not achieve the purpose of improved linearity that is achieved by the present invention using D/A converter with lower resolution.

Claim 1 has been amended to clarify the distinction over Spicer, and withdrawal of the anticipation rejection is respectfully requested, with respect to claim 1 as well as its new dependent claim 13. Claims 14 and 15 are also directed to the subject matter of Fig. 8 but are of somewhat different scope, and distinguish over the art for similar reasons.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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